

WHAT IS CLAIMED IS:

1. A slicing circuit comprising:

a control recording unit which exchanges data with a data bus;

5 a memory which temporarily stores character broadcasting data extracted from the data bus;

an A/D converter which receives a composite video signal, and converts the composite signal into digital values;

10 a digital arithmetic and logic unit which receives the digital values converted by the A/D converter, calculates character broadcasting data, and outputs the character broadcasting data to the memory;

15 a SYNC separator which receives the composite video signal, and extracts a vertical or horizontal synchronizing signal;

a clock generating unit; and

20 a timing control circuit which receives the output of the SYNC separator, clock generating unit and control recording unit, output to the memory and digital arithmetic and logic unit, and controls a timing.

2. The slicing circuit according to claim 1, wherein the digital arithmetic and logic unit includes,

25 a plurality of latch circuits;

an arithmetic processing control circuit which receives a sampling clock and a slicing clock, and outputs a first through fourth control signals that show a timing in a one-bit data width;

5           a first integrator connected to one of the plurality of latch circuits, which first integrator receives the second control signal;

10           a second integrator connected to a latch circuit, to which the first integrator is not connected, out of the plurality of latch circuits, which second integrator receives the third control signal;

            a first adder which receives the output of the first and second integrators;

15           a third integrator connected to a latch circuit, to which the first and second integrators are not connected, out of the plurality of latch circuits, which third integrator receives the first control signal;

            a second adder which receives the output of the third and first adders; and

20           a correcting circuit which receives the output of the second adder and the fourth control signal.

3.       The slicing circuit according to claim 1, wherein the digital arithmetic and logic unit includes,

25           a plurality of latch circuits;

an arithmetic processing control circuit which receives a sampling clock and a slicing clock, and outputs a first through fourth control signals that show a timing in a one-bit data width;

5        a first selector connected to at least two latch circuits out of the plurality of latch circuits, which first selector receives the first control signal;

10        a second selector connected to at least two latch circuits, to which the first selector is not connected, out of the plurality of latch circuits, which second selector receives the second control signal;

      a first adder which receives the output of the first and second selectors;

15        an integrator connected to at least two latch circuits, to which the first and second selectors are not connected, out of the plurality of latch circuits;

      a second adder which receives the output of the integrator and first adder; and

20        a correcting circuit which receives the output of the second adder.

4.    A slicing circuit for arithmetically correcting character broadcasting data extracted from a composite video signal, the slicing circuit comprising:

25        an arithmetic processing unit which changes over an

arithmetic processing at a sampling timing of the composite video signal.

Year	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100
1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100	